

INSTRUCTIONS FOR TEST & SET WITH SELECTIVELY ENABLED CACHE INVALIDATE

Abstract

5 A method and system for selectively enabling a cache-invalidate function
supplement to a resource-synchronization instruction such as test-and-set. Some
embodiments include a first processor, a first memory, at least a first cache between the
first processor and the first memory, wherein the first cache caches data accessed by the
first processor from the first memory, wherein the first processor executes: a resource-
10 synchronization instruction, an instruction that enables a cache-invalidate function to be
performed upon execution of the resource-synchronization instruction, and an
instruction that disables the cache-invalidate function from being performed upon
execution of the resource-synchronization instruction.

15

"Express Mail" mailing label number: EL671642548US

20 Date of Deposit: October 24, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37
CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.